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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,556	04/08/2004	Oscar Ming Kin Law	00100.04.0002	8355

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
07/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/820,556	KIN LAW, OSCAR MING	
	Examiner	Art Unit	
	QUAN TRA	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10 and 12-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-10 and 12-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/14/07 has been entered.

Claim objection

Claim 3 is objected because there is no antecedent basis for the limitation "the frequency monitor"

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-10 and 12-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh et al. (USP 6380764) in view of Miyazaki et al. (USP 6774705), previously cited.

As to claim 1, Katoh et al.'s figure 12 shows a delay circuit (inv1 and inv2) having first and second computing devices, each of the computing devices having different one of a plurality of different threshold voltages. Figure 12 fails to teach circuit that controls the delay time of the delay circuit. However, Miyazaki et al.'s figure 14 shows a delay control circuit (all elements excepting LSI) having circuit MON that replicates the delay circuit LSI and the remaining circuits detect and adjust the delay of both LSI and MON circuit to meet a desired delay value. Therefore, it would have been obvious to one having ordinary skill in the art to use Miyazaki et

al.'s delay control circuit to control the delay of Katoh et al.'s delay circuit (INV1 and INV2) in order to have more flexibility to select a desired delay value. Thus, the modified Katoh et al.'s figure 12 shows: a master controller (Miyazaki's OP and DCE); a dynamic voltage supplier (Miyazaki's VDDGEN); an adaptive body biaser (Miyazaki's VBBGEN); plurality of computing devices (Katoh's INV1 and INV2 in Miyazaki's MON), each of the computing devices having different one of plurality of different threshold voltages, connect and function as claimed.

As to claim 3, the modified Katoh et al.'s figure 12 shows that the frequency monitor (Miyazaki's CMP) generates a frequency offset value.

As to claim 4, the modified Katoh et al.'s figure 12 shows that the frequency offset value is based on a comparison of the output frequency indicator and a reference frequency indicator (REF).

As to claim 5, the modified Katoh's figure 12 shows that the frequency offset value is provided to the master controller (Miyazaki's OP and DEC), the master controller generating a second supply voltage indicator and a second body bias indicator in response to the frequency offset value and the operation state value, the master controller operative to provide the second supply voltage indicator to the dynamic voltage supplier and operative to provide the second body bias indicator to the adaptive body bias circuit.

As to claim 6, the modified Katoh's figure 12 shows that the plurality of computing devices operative to receive a second supply voltage from the dynamic voltage supplier and a second body bias voltage from the adaptive body biaser.

As to claim 7, the modified Katoh's figure 12 shows that the master controller receives the operation state value from a processing device (circuit that generates Miyazaki's REF).

As to claim 8, the modified Katoh's figure 12 shows that the plurality of computing devices are disposed on a processing element.

As to claim 9, the modified Katoh's figure 12 shows that the supply voltage indicator and the body bias indicator are voltages.

Claims 10 and12-19 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

As to claims 20 and 22-23, the modified Katoh's figure 12 shows first and second sub-section (INV1 and INV2 in Miyazaki's MON), each sub-section includes a plurality of computing devices (PMOS and NMOS) having different one of a plurality of threshold voltages relative to the other sub-sections.

As to claim 24, the modified Katoh's figure 12 further shows that the plurality of computing devices comprises a first computing device (INV1) and a second computing device (INV2) comprises at least two transistor devices operatively coupled in a push-pull configuration, and an output of the first computing device is coupled to an input of the second computing device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUAN TRA whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, ROBERT J. PASCAL can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

QUAN TRA
PRIMARY EXAMINER
Art Unit 2816

June 27, 2007